WHAT IS CLAIMED IS:

1. A semiconductor device comprising:

a) a semiconductor substrate;

b) a first region of a first conductivity type in the semiconductor substrate;

c) a second region of a second conductivity type in the semiconductor substrate;

d) a plurality of charge control electrodes, wherein each charge control electrode in the plurality of charge control electrodes is adapted to be biased differently than other charge control electrodes in the plurality of charge control electrodes; and

e) a dielectric material disposed around each of the stacked charge control electrodes.

2. The semiconductor device of claim 1 wherein the semiconductor device is a power diode.

3. The semiconductor device of claim 1 wherein the semiconductor device is a bipolar transistor.

4. The semiconductor device of claim 1 wherein the semiconductor substrate comprises a trench and wherein the charge electrodes in the plurality of charge control electrodes are stacked within the trench.

5. The semiconductor device wherein the plurality of charge control electrodes is a first plurality of charge control electrodes and wherein the semiconductor device includes a second plurality of charge control electrodes.

6. The semiconductor device of claim 1 wherein the first conductivity type is n-type and the second conductivity type is p-type.

7. The semiconductor device of claim 1 wherein the each of the plurality of charge control electrodes comprise polysilicon.

8. The semiconductor device of claim 1 wherein the plurality of charge control electrodes are biased to produce a generally uniform electric field in the first region.

9. A field effect transistor comprising:

a) a semiconductor substrate of a first conductivity type having a major surface, a drift region, and a drain region;

b) a well region of a second conductivity type formed in the semiconductor substrate;

c) a source region of the first conductivity type formed in the well region;

d) a gate electrode formed adjacent to the source region;

e) a plurality of stacked charge control electrodes buried within the drift region, wherein each charge control electrode of the plurality of stacked charge control electrodes is adapted to be biased differently than other charge control electrodes in the plurality of charge control electrodes; and

f) a dielectric material disposed around each of the stacked charge control electrodes.

10. The field effect transistor of claim 9 wherein the plurality of stacked charge control electrodes is directly under the gate electrode.

11. The filed effect transistor of claim 9 wherein the gate electrode is a trenched gate electrode.

12. The field effect transistor of claim 9 further comprising a plurality of biasing elements capable of respectively biasing the control electrodes within the plurality of control electrodes.

13. The field effect transistor of claim 9 wherein the plurality of stacked control electrodes is disposed to a side of the gate electrode.

14. The field effect transistor of claim 9 wherein the plurality of stacked control electrodes are a first plurality of stacked control electrodes, and wherein the field effect transistor further includes a second plurality of stacked control electrodes.

15. The field effect transistor of claim 9 wherein the plurality of stacked charge control electrodes is adapted to adjust an electrical field profile within the drift region of the semiconductor substrate so that the magnitude of the electrical field throughout the drift region is generally uniform and exceeds 2×10^5 V/cm.

16. The field effect transistor of claim 9 further comprising a trench, wherein the charge control electrodes within the plurality of stacked control electrodes are disposed within the trench.

17. The field effect transistor of claim 9 wherein the field effect transistor is a power metal oxide semiconductor field effect transistor (MOSFET).

18. A method for forming a semiconductor device, the method comprising:

a) providing a semiconductor substrate having a first region of a first conductivity type;

b) forming a region of a second conductivity type in the semiconductor substrate;

c) forming a first charge control electrode; and

d) forming a second charge control electrode, wherein the first charge control electrode is adapted to be biased differently than the first charge control electrode.

19. The method of claim 18 further comprising forming a trench in the semiconductor substrate and wherein forming the first charge control electrode comprises depositing a conductive material in the trench and then etching the deposited conductive material.

20. The method of claim 19 wherein the conductive material is a first conductive material and wherein forming the second charge control electrode comprises depositing a second conductive material in the trench and then etching the deposited second conductive material.

21. The method of claim 18 further comprising:

forming a trenched gate structure in the semiconductor substrate.

22. The method of claim 18 wherein the first and second charge control electrodes comprise polysilicon.

23 . The method of claim 18 wherein the method further comprises forming a plurality of biasing elements on or in the semiconductor substrate, wherein the biasing elements are adapted to bias the first and second charge control electrodes at different voltages.

24. The method of claim 18 wherein the semiconductor device is a power MOSFET.

25. A field effect transistor comprising:

a) a semiconductor substrate of a first conductivity type having a major surface, a drift region, and a drain region;

b) a well region of a second conductivity type formed in the semiconductor substrate;

c) a source region of the first conductivity type formed in the well region;

d) a source contact layer coupled to the source region;

e) a gate electrode formed adjacent to the source region;

f) a charge control electrode buried in the drift region, wherein the charge control electrode is adapted to be biased at a different potential than the gate electrode or the source contact layer, and is adapted to control the electric field in the drift region; and

g) a dielectric material disposed around the charge control electrode.

26. The field effect transistor of claim 25 further comprising a biasing element adapted to bias the charge control electrode at the different potential.

27. The field effect transistor of claim 25 wherein the gate electrode is a trenched gate electrode.

28. The field effect transistor of claim 25 wherein the charge control electrodes is directly under the gate electrode.

29. The field effect transistor of claim 25 wherein the charge control electrode is directly under the gate electrode and wherein the gate electrode is a trenched gate electrode.

30. A method for forming a field effect transistor comprising:

a) providing a semiconductor substrate of a first conductivity type having a major surface, a drift region, and a drain region;

b) forming a well region of a second conductivity type in the semiconductor substrate;

c) forming a source region of the first conductivity type in the well region;

d) forming a source contact layer on the source region;

e) forming a gate electrode adjacent to the source region;

f) forming a charge control electrode in the drift region, wherein the charge control electrode is adapted to be biased at a different potential than the gate electrode or the source contact layer, and is adapted to control the electric field in the drift region; and

g) forming a dielectric material around the charge control electrode.

31. The method of claim 30 wherein the gate electrode is a trenched gate electrode.

32. The method of claim 30 further comprising:

forming a biasing element, wherein the biasing element is adapted to bias the charge control electrode.